

REMARKS

In response to the Examiner's Action mailed October 4, 2002, Applicants amend their application and request reconsideration. No claims are added or cancelled so that claims 18-25 remain pending.

In this Amendment claim 18 is amended at two locations. In the second of those locations, there is merely a clarifying amendment so that there is a reduced probability of confusion in correlating which insulating regions are under which bending positions of the first and second gate electrodes. There is no change in the scope of the claim. The second amendment, discussed in the following paragraph, responds to the rejection as to form.

The claims were rejected as not supported by the original patent application, pursuant to 35 USC 112, first paragraph, because of an alleged failure to support the phrase "an anisotropic compound semiconductor substrate" in the first words of the first paragraph of the claim. The rejection has been overcome by removing the words "an anisotropic" from that phrase. The compound semiconductor substrate is described in the patent application and in the first paragraph of claim 18 as being "electrically isotropic in two mutually orthogonal directions". The exemplary substrate material described in the patent application is gallium arsenide and persons of skill in the art recognize that that material is electrically isotropic in two mutually orthogonal directions. Those persons also recognize that this property and this description of the property means that gallium arsenide is, in many characteristics, anisotropic.

All pending claims were rejected as unpatentable over Tsutsui (U.S. Patent 5,925,901) in view of Taguchi (U.S. Patent 5,001,108), Tozawa (JP 3-270024) and Kobayashi (JP 61-232682).¹ This rejection is respectfully traversed.

It is fundamental that one of the two prerequisites for establishing *prima facie* obviousness is that the prior art references relied upon must disclose all of the elements of a claim so rejected. Even if all of the elements of a claim are disclosed in the hypothetical combination of prior art publications, motivation for the combination must also be established to demonstrate *prima facie* obviousness. The rejection here fails the first of these two essential tests.

Key features of the semiconductor device described in claim 18 are the presence of first, second, and third active regions on the first surface of the substrate, the first and second active regions being separated by a first insulating region and the second and third active region being

¹ As previously indicated, Taguchi is not relevant because it concerns a superconducting field effect transistor. Further, Taguchi is unnecessary to the rejection, having been cited as describing "an anisotropic compound semiconductor substrate". GaAs is a compound semiconductor substrate within the scope of claim 18, and Tsutsui employs a GaAs substrate, demonstrating that, if Taguchi is pertinent to the claims, it is, at best, cumulative to Tsutsui.

separated by a second insulating region. This structure is particularly important because it gives meaning to the final lines in claim 18. Those lines specify that the first insulating region is under the first and third bending positions of the first and second gate electrodes and the second insulating region is under the second and fourth bending positions of the first and second gate electrodes. No publication relied upon in rejecting the claims discloses these key elements of the claims and therefore *prima facie* obviousness cannot be demonstrated by relying upon the purported combination of references.

At page 4 of the Official Action, the Examiner compared the language of the first and second paragraphs of claim 1 to Tsutsui and Taguchi although, as noted, Taguchi is not essential to this comparison. Applicants do not question the comparison of the first paragraph of claim 18 to either reference and acknowledge that Tsutsui describes a compound semiconductor substrate as in the first paragraph of claim 18. However, the comparison of Tsutsui to the second paragraph of claim 18 is simply incorrect.

According to the Official Action,

first [,] second [,] and third active regions on the first surface of the substrate (Tsutsui fig. 1), the first and second active regions being separated by a first insulating region (Tsutsui col. 4 lines 30-34) and the second and third active regions being separated by a second insulating region. (Tsutsui fig. 1)....

Tsutsui does not disclose any such structure. While reference is made in the cited passage of the Official Action to Figure 1 of Tsutsui, the passage at column 4, lines 30-34 of Tsutsui refers to Tsutsui's Figure 7. The structure shown in those two figures of Tsutsui are, in pertinent part, identical. Each of the structures includes a single active region 2. This fact is not only observable from those Figures 1 and 7, but is explicitly described in the text of Tsutsui. Figure 1 is described in column 1, lines 22-26, where Tsutsui states that "an active region 2 [is] formed in the surface portion of the substrate by ion implantation." Inspection of Figure 1 shows that there is a single such active region 2 extending across the semiconductor substrate. Column 4, lines 30-31 of Tsutsui state that the "active region 2 is surrounded by an insulation region formed by ion implantation" Reference to Figure 7 shows that that figure depicts, like Figure 1, a single active region 2 extending across the width of the substrate of the substrate. There is no description anywhere within the specification of Tsutsui of multiple active regions. Thus, on this first ground, the comparison of Tsutsui to claim 18 is flawed.

Because there are no multiple active regions in the Tsutsui structure, there can be no first and second insulating regions that separate respective parts of the first, second, and third active regions from each other. The statement in the Official Action to the contrary finds no support in

the prior art. Because these additional elements of the claimed structure are missing from the prior art, the comparison is, for a second reason, erroneous and the rejection incorrect.

Reliance was placed upon Tozawa with regard to gate electrodes bent at bending positions. That limited disclosure is present in Tozawa. At page 6 of the Official Action, in lines 11-14, the Examiner asserts that the limitation described in the final lines of claim 18 is present within the prior art, focusing attention on Figure 1A of Tozawa. According to the Official Action, in "Tozawa fig. 1A, electrodes 1 and 3 and regions between the electrodes" are the insulating regions of the final paragraph of claim 18. This comparison is incorrect on three independent grounds.

First, the final paragraph of claim 18 refers to the bending positions of gate electrodes. The electrodes 1 and 3 in Tozawa are source and drain electrodes, not gate electrodes. Thus, the comparison is inappropriate.

Second, what the regions in Tozawa *between* the source and drain electrodes of 1 and 3, regions including the gate electrodes 2, might be, is not disclosed by Tozawa. Assuming there is electrical insulation in those regions, the claim limitation is still not met. Claim 18, as examined and as pending here refers to the first and second insulating regions as being *under* the bending positions of the first and second gate electrodes, not *between*. The difference is important and demonstrates a further error in the rejection.

Third, of course, since neither Tsutsui nor Tozawa describes multiple active regions, pairs of which are separated by respective insulating regions, it would be impossible for any combination of those references to include all of the elements of the final paragraph of claim 18 anyway. Based upon any of these grounds, the rejection is as erroneous with respect to its assertion that the elements of the final paragraph of claim 18 are found in the prior art.

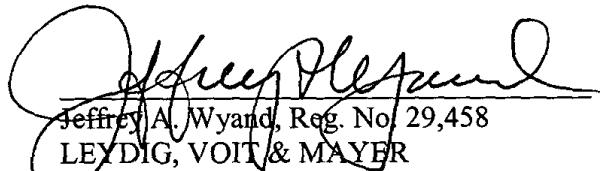
In summary, the rejection of claim 18 is erroneous because no reference discloses the elements of the second and final paragraphs of that claim. Either of these failings, for any of the multiple reasons supplied for each failing, is sufficient for withdrawal of the rejection.

Claims 19-25 are all dependent claims depending directly or indirectly from claim 18. The rejection of those claims relies upon no additional references and is founded upon the assertion that claim 18 is obvious in view of the combination of four references. Since, for the reasons explained in detail above, *prima facie* obviousness has not been demonstrated with respect to claim 18, *prima facie* obviousness has likewise not been demonstrated with respect to claims 19-25. Therefore, further comment on the rejection of the dependent claims is unnecessary.

In re Appln. of SUZUKI et al.
Application No. 09/613,749

In view of several errors in the rejection, upon reconsideration, all of claims 18-25 should be allowed.

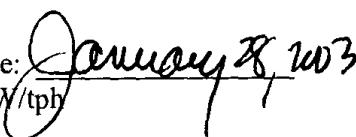
Respectfully submitted,



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PATENT
Attorney Docket No. 400762/AOYAMA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SUZUKI et al.

Application No. 09/613,749

Art Unit: 2814

Filed: July 11, 2000

Examiner: A. Rao

For: **FIELD EFFECT TRANSISTOR
STRUCTURE WITH BENT GATE**

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**AMENDMENTS TO CLAIMS
MADE IN RESPONSE TO OFFICE ACTION DATED OCTOBER 4, 2002**

Amendments to existing claims:

18. (Amended) A semiconductor device comprising:

~~An anisotropic~~ a compound semiconductor substrate having a first surface and a second surface, the compound semiconductor substrate being electrically isotropic in two mutually orthogonal directions;

first, second, and third active regions on the first surface of the substrate, the first and second active regions being separated by a first insulating region and the second and third active regions being separated by a second insulating region;

a first semiconductor element including

first, second, and third channel regions serially connected, adjacent channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first, second, and third channel regions and opposing each other with the first, second, and third channel regions therebetween, and in ohmic contact with the first, second, and third active regions, and

a first gate electrode disposed on the first, second, and third channel regions and along the first source electrode and the first drain electrode, and bent at first and second bending positions; and

a second semiconductor element on the first, second, and third active regions adjacent to the first semiconductor element, including

fourth, fifth, and sixth channel regions serially connected, adjacent channel regions having width directions essentially perpendicular to each other, the fourth, fifth, and

sixth channel regions being adjacent to the first, second, and third channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

a second source electrode and a second drain electrode in ohmic contact with the first, second, and third active regions, one of the second source electrode and the second drain electrode and opposing the first drain electrode or the first source electrode across the fourth, fifth, and sixth channel regions, and

a second gate electrode on the fourth, fifth, and sixth channel regions and along one of the second source electrode and the second drain electrode, and bent at third and fourth bending positions, wherein the ~~first and second insulating regions are~~ region is under the first and third bending positions of the first and second gate electrodes, and the second insulating region is under the second and fourth bending positions of the first and second gate electrodes, respectively.